SPECIFICATION

Please amend the Specification as follows:

Please replace the first paragraph beginning on Page 5 with the following:

FIGURE 1 presents a high level representation of a portion 10 of a typical general purpose computer or CPU. An instruction cache 12 fetches instructions from some type of storage (not shown). These instructions are decoded in a block 14 and are issued, via an issue block 16 and a bus 18, to a plurality of execution units 20, 22, 24 and 26. It may be noted that issue block 16 also contains an MSR (Machine State Register) block not numerically designated but discussed later in connection with FIGURE 2. The first designated execution unit 20 is shown as a SIMD (Single Instruction Multiple Data stream) VMX (Vector Multimedia Execution) device which comprises a vector register file unit, or VRF, as well as arithmetic subunits designated as 28, 30, 32 and 34. Subunit block 28 is further designated as VMX SIM or simple fixed point subunit. Subunit block 30 is further designated as VMX PER or permute subunit. The subunit block 32 represents a COM or complex fixed point subunit, while subunit block 34 represents a single precision FPU (Floating Point Unit). The second execution unit 22 is a scalar FPU and comprises an FPR (Floating Point Register file) portion and a double precision FPU pipeline portion further designated as FPU. The third execution unit block 24 is a fixed point unit including, as shown, a GPR (General Purpose Register) portion, an FXU (Fixed ~~(Point~~ Point Subunit) portion including an ALU (Arithmetic/Logical Subunit) portion, an LSU (Load/Store) portion and a DC (Data Cache) portion. A bus 36 connects each of the first three execution units to other parts of the computer, such as computer memory. A bus 38 connects the DC (Data Cache) portion of block 24 to the instruction cache 12 as well as to an L2 cache interface 40. The cache 40 is interconnected to other chip components of the computer via a chip bus designated as MPI Bus. The remaining block 26 comprises a branch processing unit including CR (Condition Code Register), LR (Link Register) and CTR (Count Register) portions as well as a CR logic subunit and a BR (Branch) processing subunit. The various portions of block 26 interact with blocks 20, 22 and 24 to process the instructions.